Multi-rate Polyphase DSP and LMS Calibration Schemes for Oversampled Data Conversion Systems

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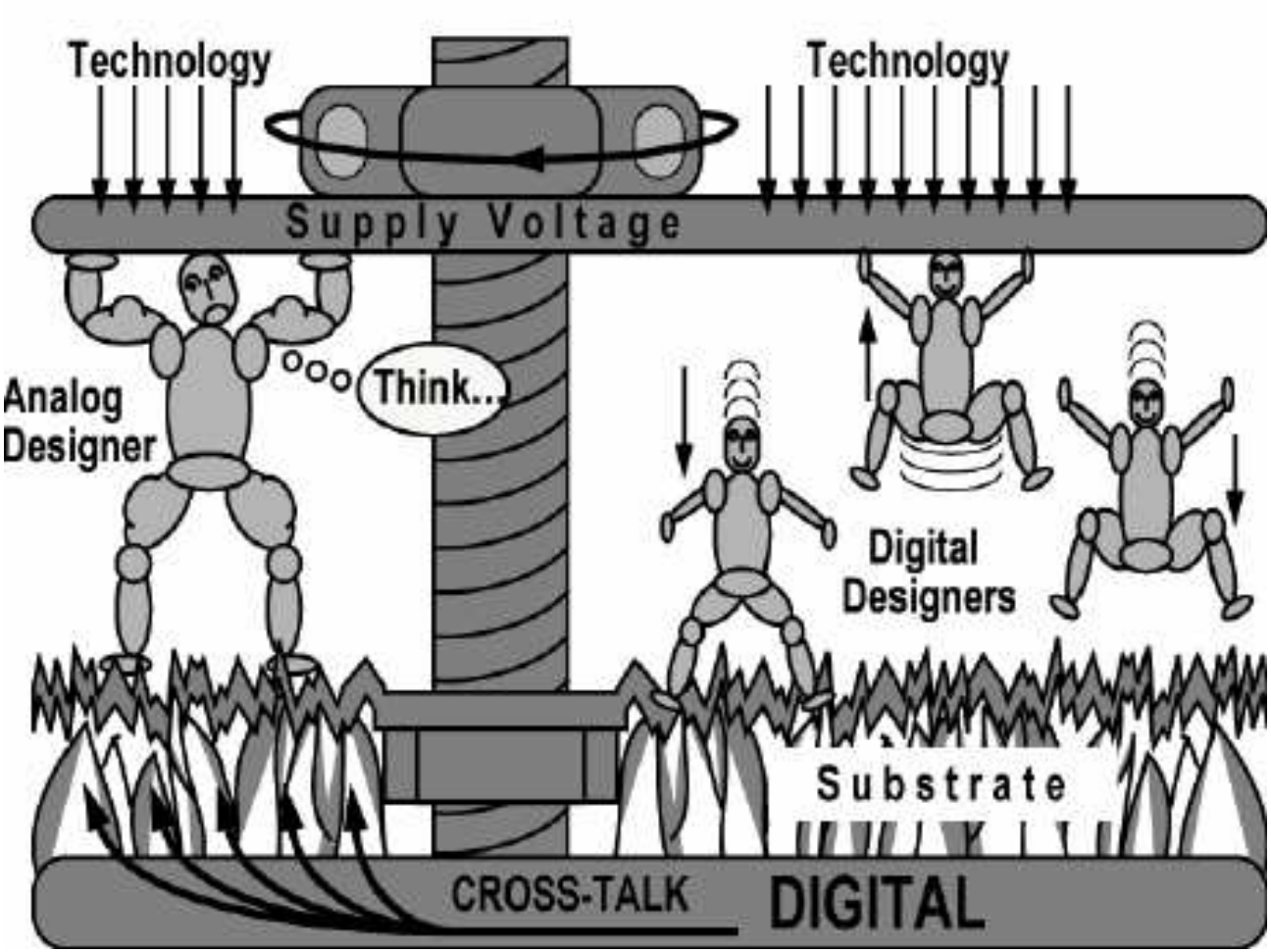
Outline

- Motivation: Digitally-assisted Analog Circuits
- Brief Overview of ΣΔ ADC
- Proposed Low-gain LMS-Calibrated ADC
- Proposed Multi-Rate LMS Decimation Filter
- Conclusions

Digitally-Assisted ADCs



* Prof. A. Sangiovanni-Vincentelli, UC, Berkeley

- Low voltage headroom
- Wide bandwidth–high sampling frequencies
- Use digital to correct analog imperfections!

ADCs – General Overview

ADCs	Throughput	Resolution	Latency	Power	Area
Flash	👍👍👍👍	👎	👍👍👍👍	👎	👍👍
Pipeline	👍👍👍	👍👍	👍👍	👍👍	👍👍👍
SAR	👍👍	👍👍👍	👎	👍👍👍👍	👎
Sigma-Delta (ΣΔ)	👍👍	👍👍👍👍	👍👍👍	👍👍👍	👍👍👍👍

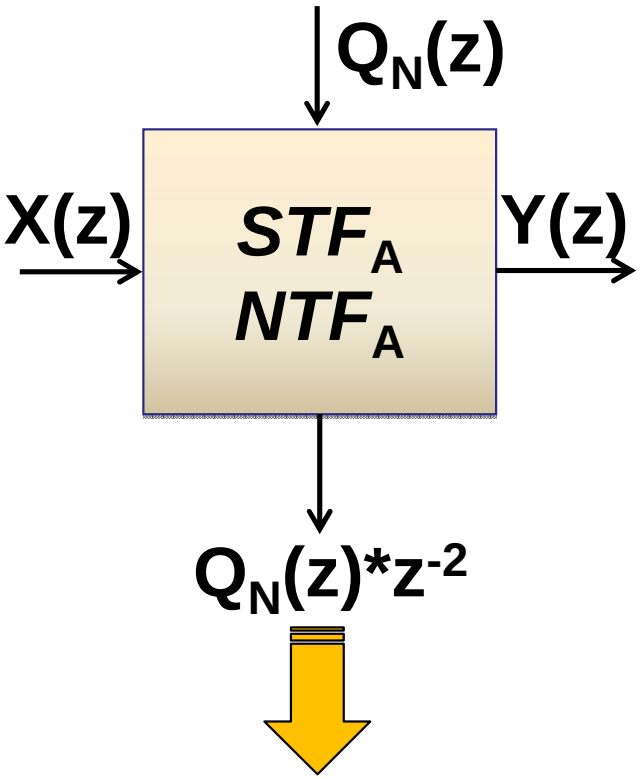
- **ΣΔ ADCs most suitable for low/medium bandwidth, high-resolution applications**
- **Requirement:**
  - **9.5 MHz BW, 11b effective number of bits (ENOB)**

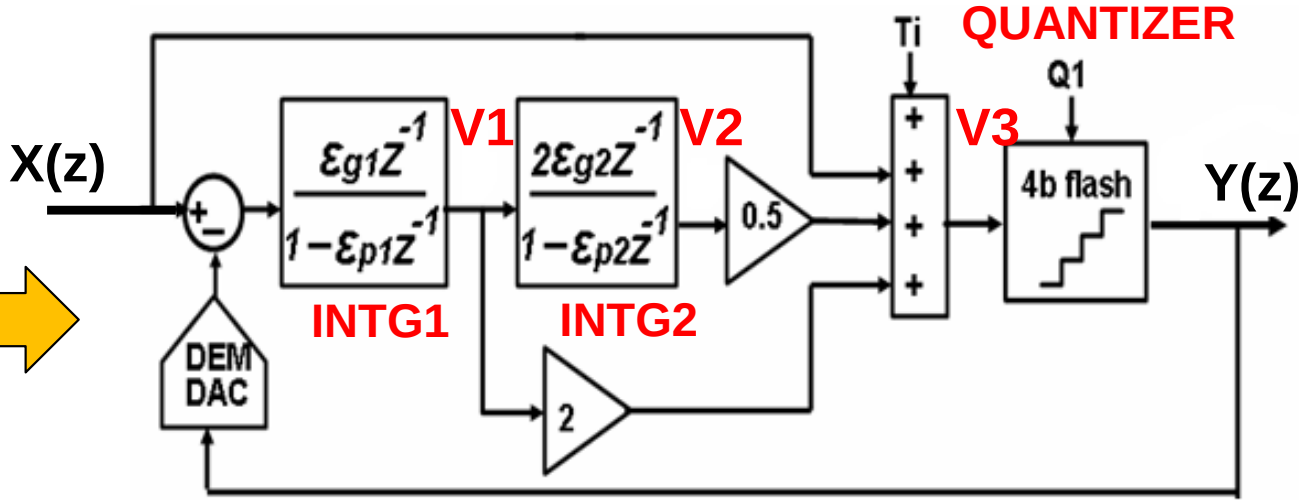
Implementation Choices

- **Over-sampling ratio = OSR = $f_s/2f_b$**
  - **f_s = sampling frequency, f_b = signal bandwidth**
  - **Higher OSR ⟹ Higher SNR But Higher f_s as well.**
  - **Low OSR = 8 for this design**

- **How viable are designs using low-gain opamps?**
  - **ADC using 26-dB gain opamp feasible?**
  - **Digitally calibrate analog gain errors?**
  - **Power and area-efficient CMOS process?**

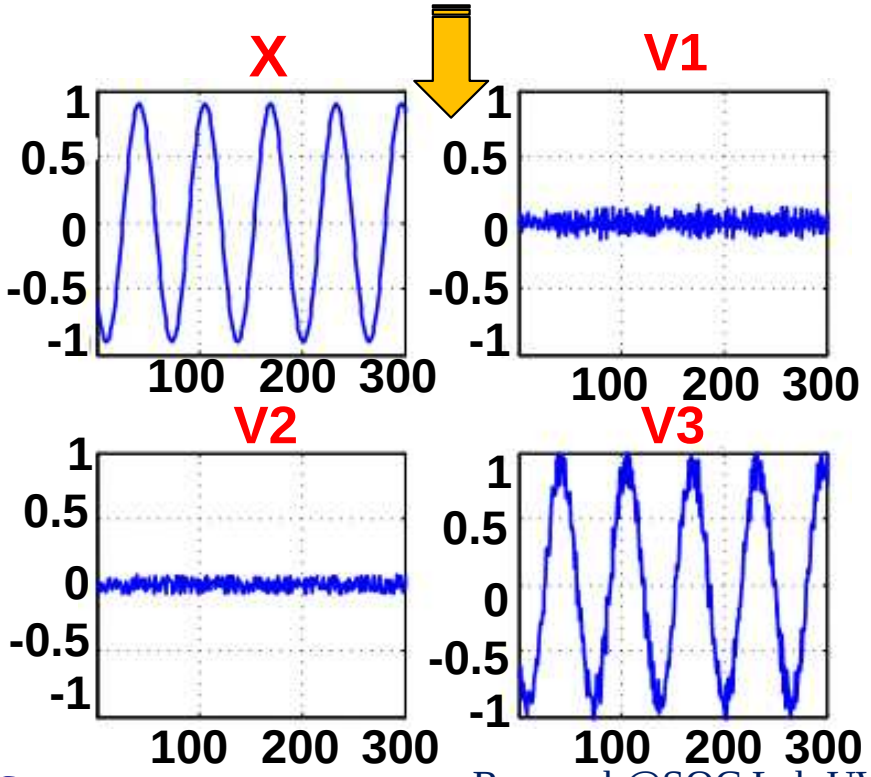
Second-order ΣΔ ADC Topology





$$STF_A(z) = 1$$
$$NTF_A(z) = (1-z^{-1})^2$$

$$Y(z) = \boxed{1}\cdot X(z) + \boxed{(1-z^{-1})^2}\cdot Q_N(z)$$
$$STF_A(z) \quad NTF_A(z)$$



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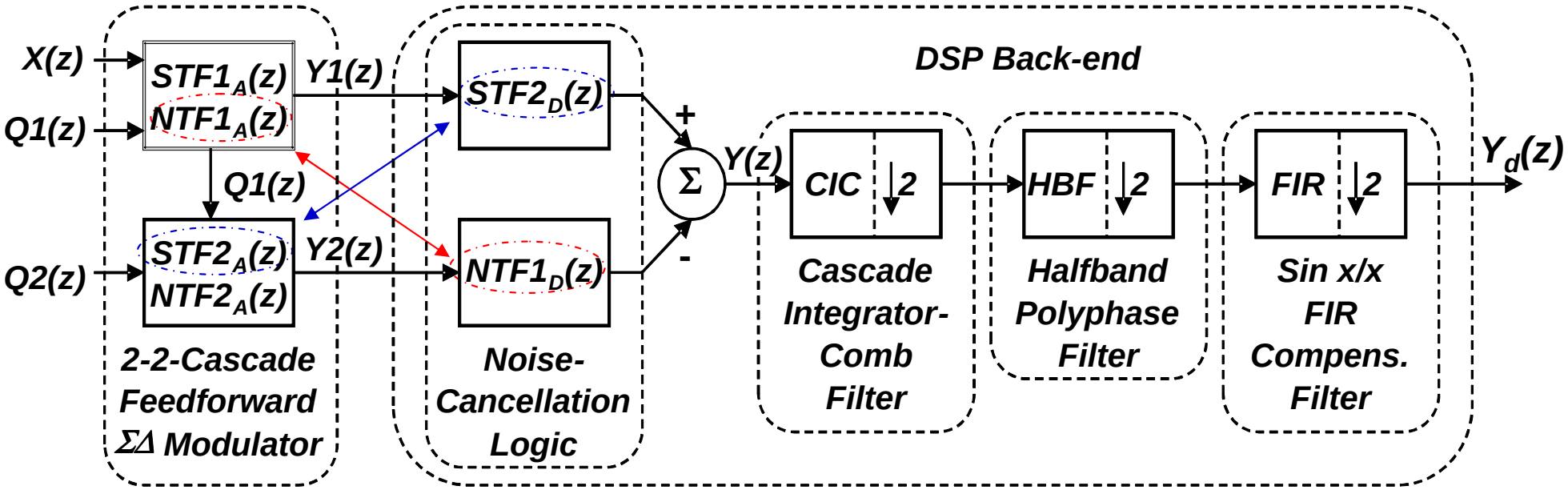
Cascade ΣΔ ADC with DSP Back-end



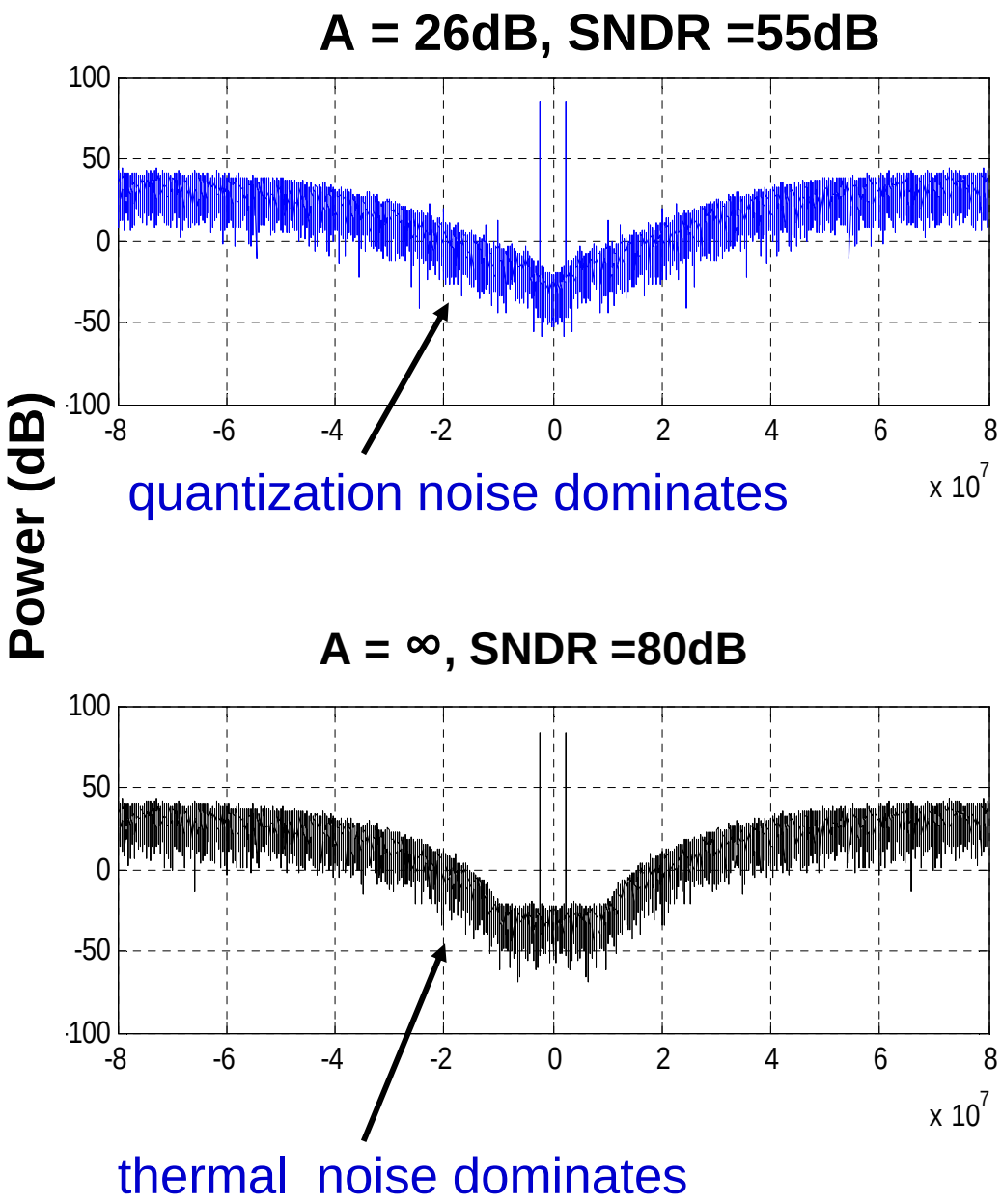
$Y(z) = STF1_A(z) \cdot STF2_D(z) \cdot X(z)$ ← Input Signal

$+ [NTF1_A(z) \cdot STF2_D(z) - NTF1_D(z) \cdot STF2_A(z)] \cdot Q_1(z)$ ← 1st-stage Quan.

$- 1/h \cdot NTF2_A(z) \cdot NTF1_D(z) \cdot Q_2(z)$ ← 2nd-stage Quan. noise

- High-order noise shaping
- Inherently stable with second-order stages
- Requires good matching of analog & digital transfer functions

Cascade ADC with 26-dB Opamp



- A_{DC}= 26 dB (20 V/V)

$$NTF1_A(z) = \frac{1.0000 - 1.8747z^{-1} + 0.8772z^{-2}}{1.0000 - 0.1754z^{-1} - 0.0063z^{-2}}$$

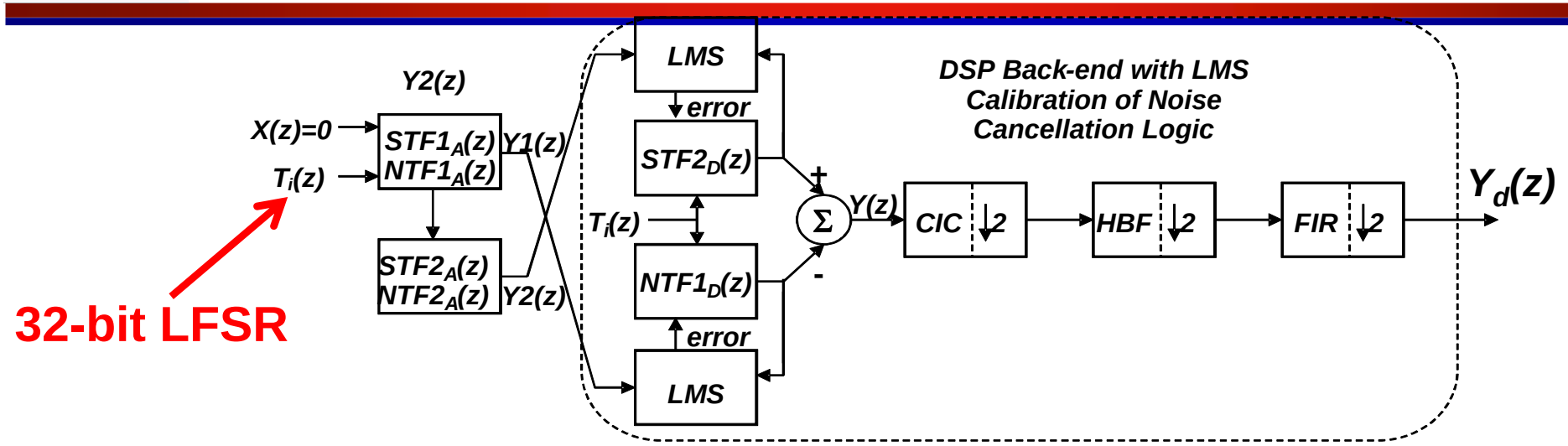
$$NTF1_D(z) = 1 - 2z^{-1} + z^{-2} = (1 - z^{-1})^{-2}$$

$$STF2_A(z) = \frac{0.7858z^{-2}}{1 - 0.1754z^{-1} - 0.0063z^{-2}}$$

$$STF2_D(z) = z^{-2}$$

- Mismatch causes Q1 leak to the output
- SNDR degrades severely.
- Capacitor mismatches & PVT variations have similar effects

Cascade ADC with Low-gain Opamps and Calibration—1



- **Calibrate $NTF1_D$ and $STF2_D$:**
  - **Input digital pseudo-random sequence T_i after X(z) is set to 0**
  - **Sign-data LMS algorithm:**

$$W(n+1) = W(n) + 2 \cdot \mu \cdot e(n) \cdot \mathrm{sgn}(T_i(n))$$

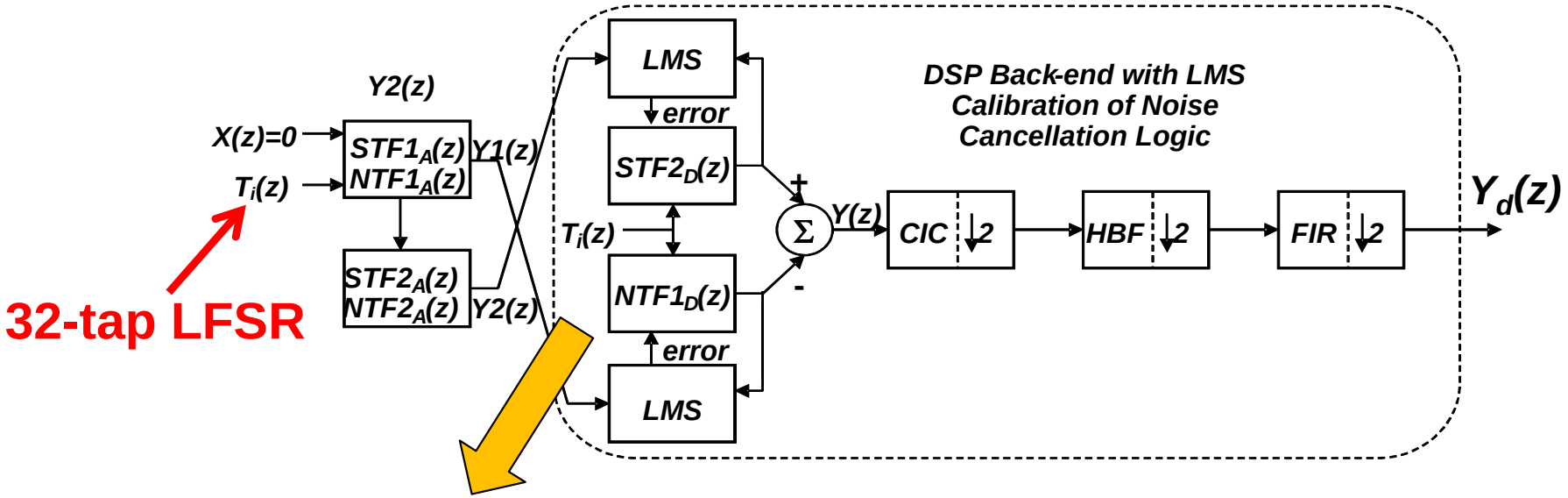
  - **Ti and Qi are uncorrelated stationary signals**

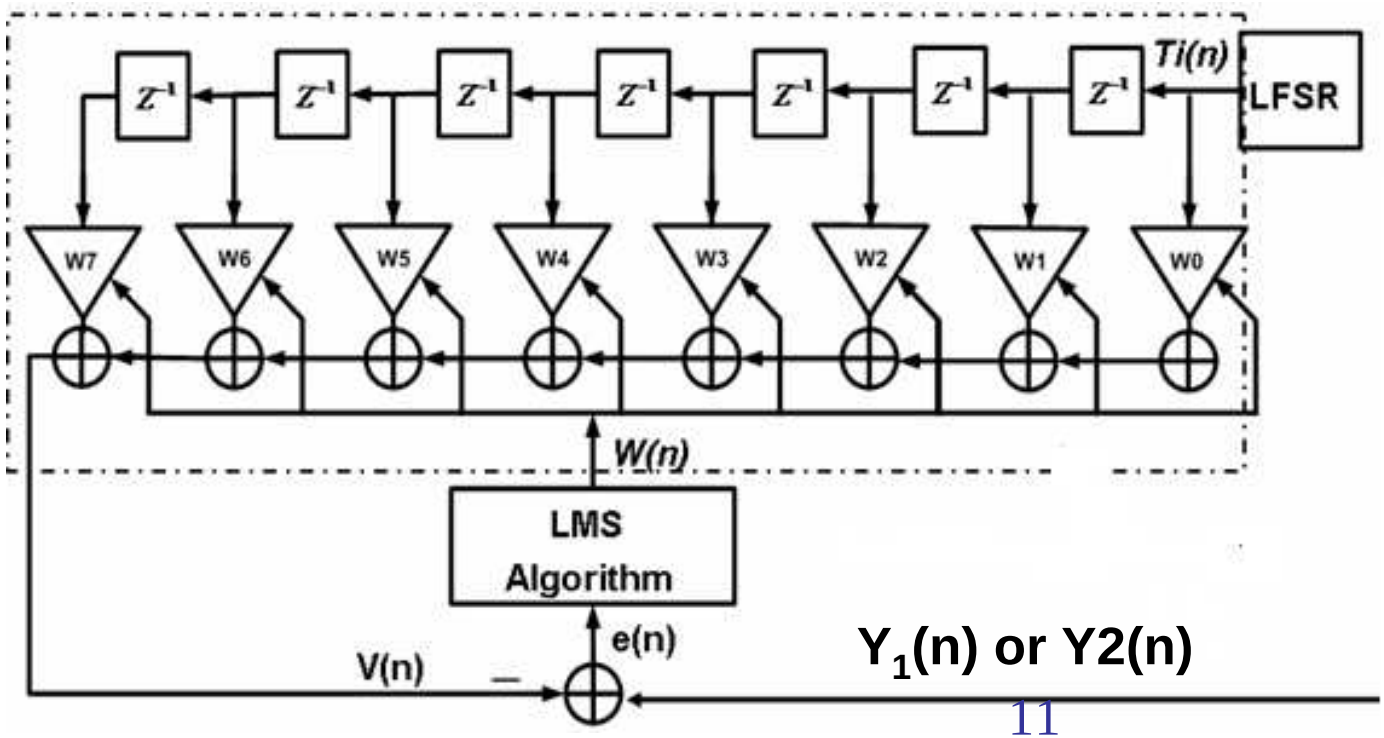
$$\frac{\partial\left(E\left[e^2(n)\right]\right)}{\partial W_o(n)} = 0$$

$$W_o(z) = \frac{\Phi_{Y_I T_I}(z)}{\Phi_{T_I T_I}(z)} = \frac{NTF1_A(z) \cdot \Phi_{T_I T_I}(z)}{\Phi_{T_I T_I}(z)} = NTF1_A(z)$$

After calibration ideally:
$STF_{2D} = STF_{2A}$
$NTF_{1D} = NTF_{1A}$

Cascade ADC with Low-gain Opamps and Calibration—2





- **8-tap FIR filter for STF_{2D}/NTF_{1D} to reduce truncation error.**
- **But, large power consumption – 3X more than analog.**

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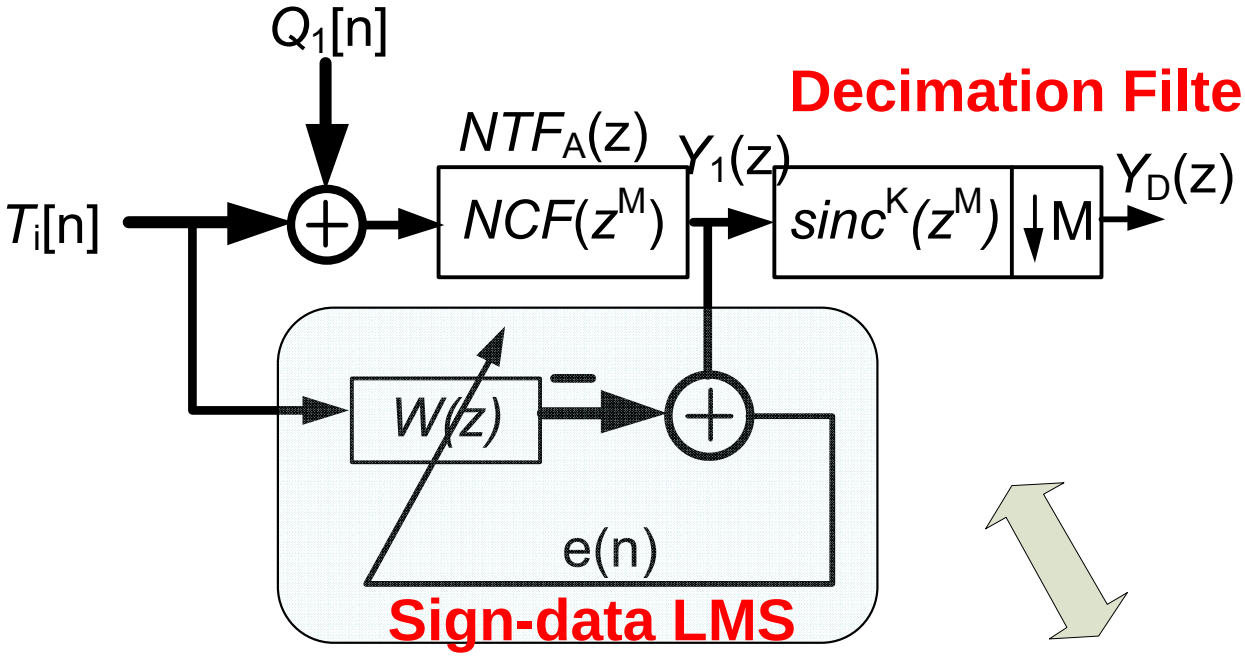
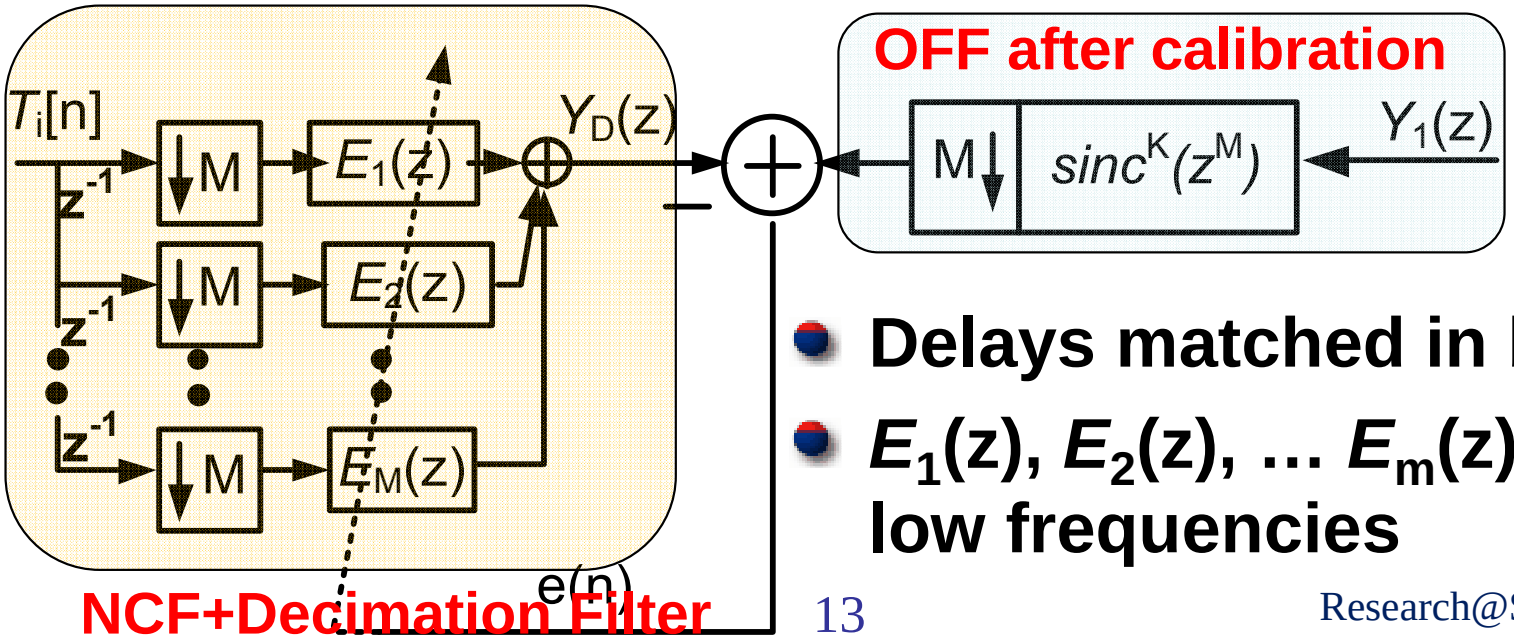
Polyphase Decomposition of LMS Calibrated NCF + Decimation Filter



Decimation Filter

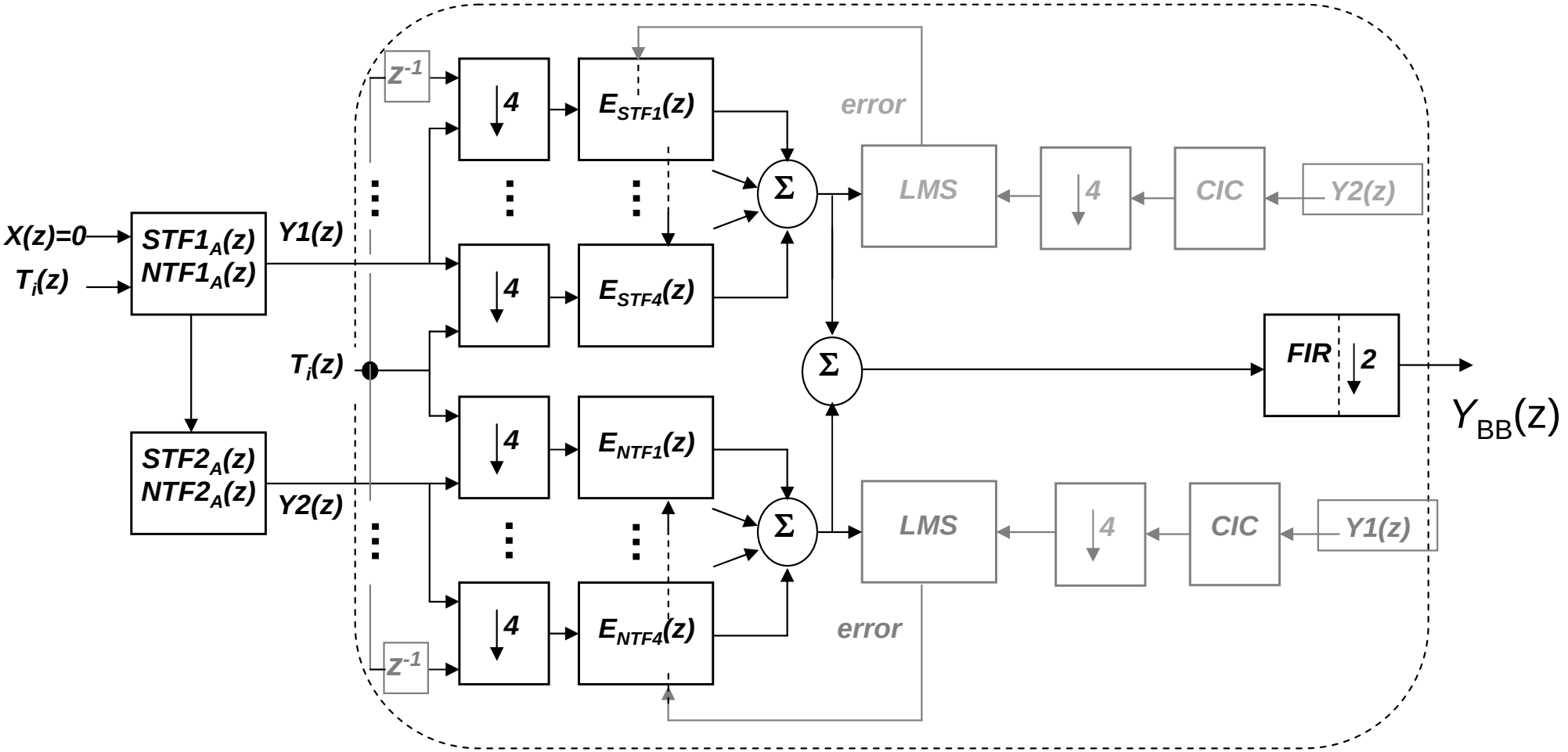
Conventional

Proposed



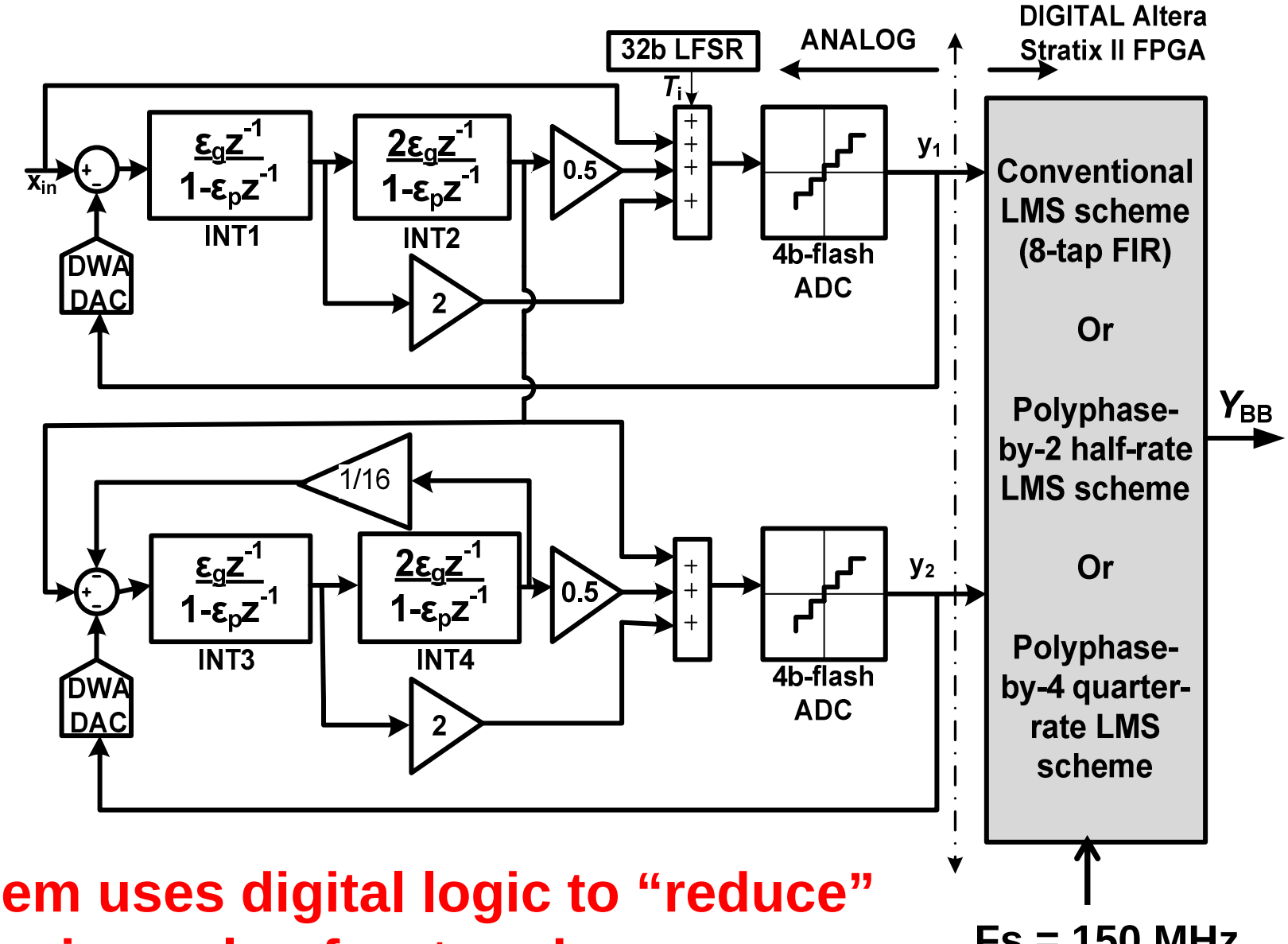
- Delays matched in both paths
- $E_1(z)$, $E_2(z)$, … $E_m(z)$ operate at low frequencies

Quarter-rate LMS



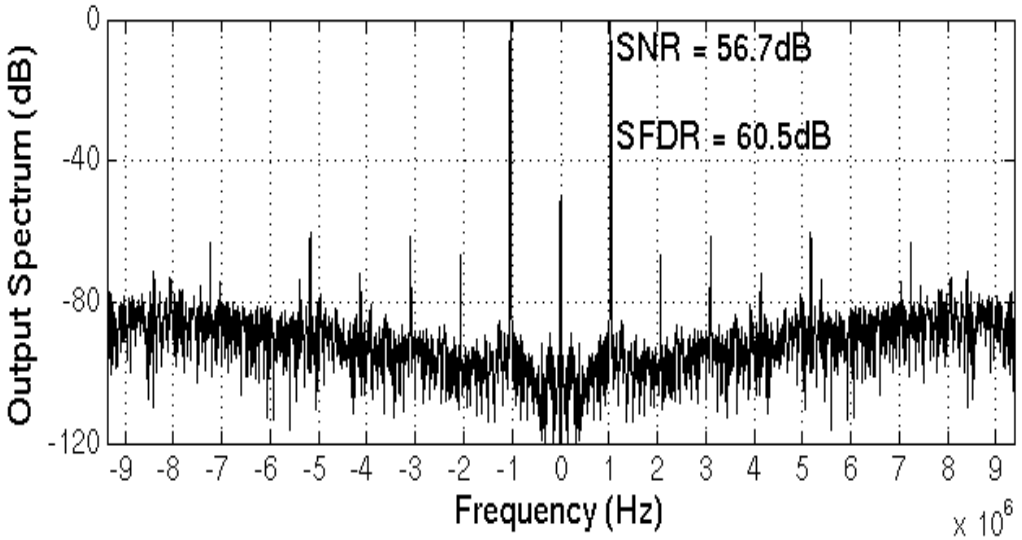
- *Simulink* HDL Coder used to generate parameterized Verilog
- Minimal area overhead due to increase in # of taps of $E_1(z)$ … $E_m(z)$ after LMS calibration. Power decreases by ~ 30%.
- Same number of data points required for offline calibration

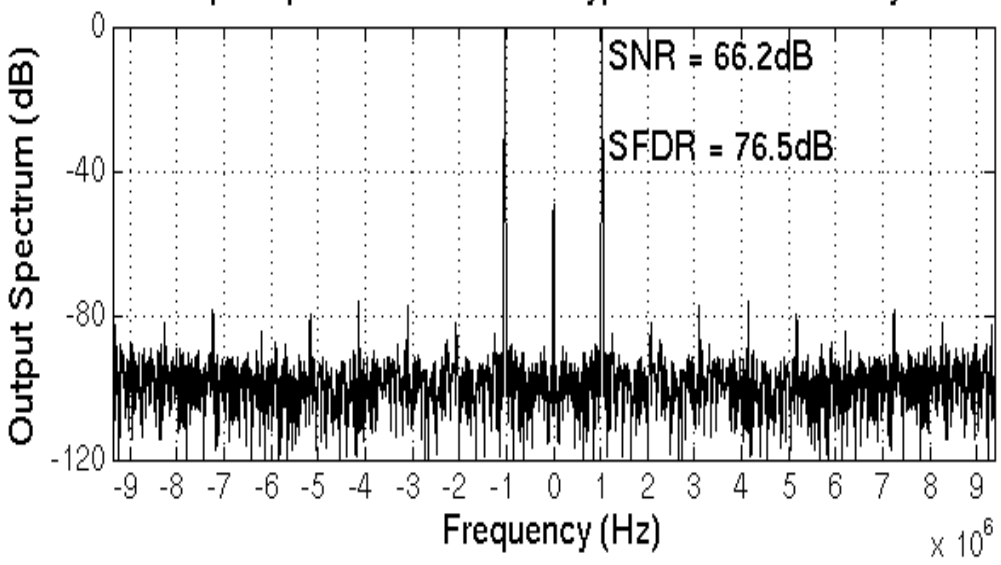
Proposed ΣΔ ADC System

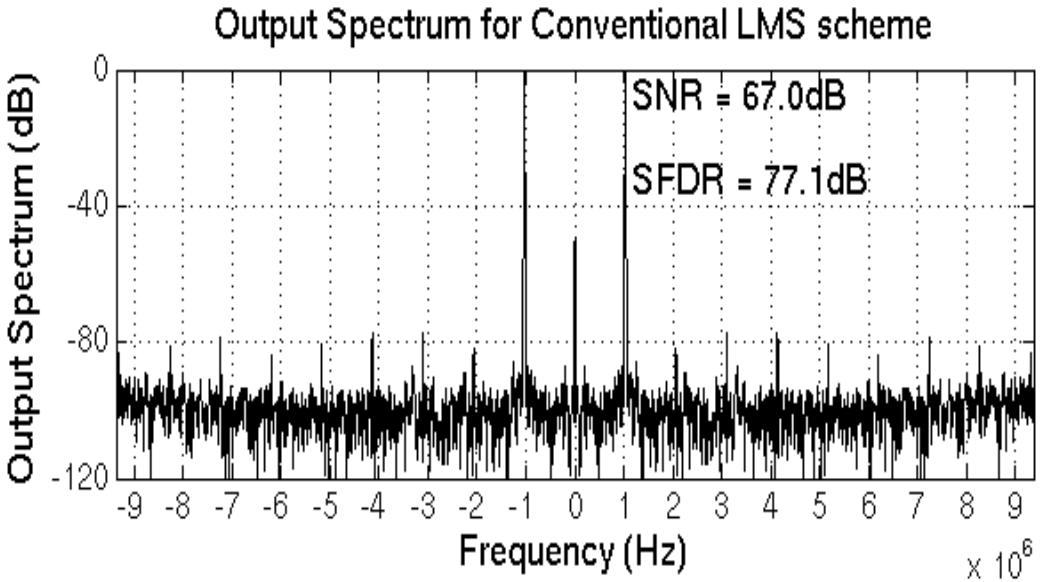


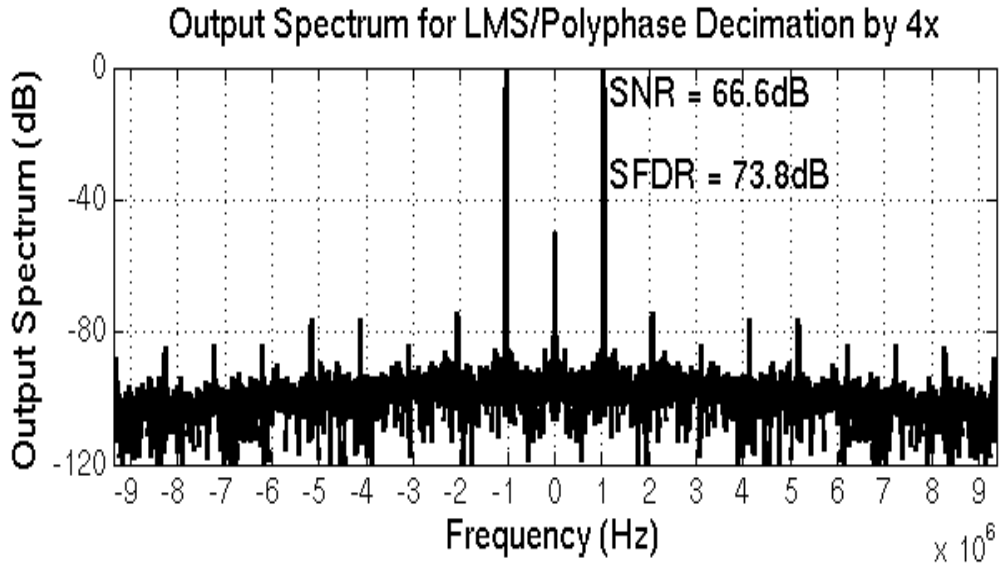
System uses digital logic to "reduce" errors in analog front-end.

Measured SNR/SFDR After Decimation









Measured Specs with Calibration

Sampling Frequency (MHz)	150
Signal Bandwidth (MHz)	9.4
Oversampling Ratio	8
Peak SNR/SNDR/SFDR (dB)	67/66/75
Input Range (Differential) (V_{p-p})	2.4
$+V_{ref}/V_{cm}/-V_{ref}$ (V)	1.2/0.6/0.0
Power Consumption (mW)	31.5
Power Supply Voltage (V)	1.25
Core Chip Area (mm^2)	1.73
CMOS Process	0.13 µm

Comparison

	THIS WORK (NO POLYPHASE)	THIS WORK (POLYPHASE 4X)	BOSI [1]	BREEMS [4]	SHU [5]
Architecture	2-2 DT	2-2 DT	2-2 CT	2-2 CT	2-1-1 CT
OSR	8	8	4	8	10
SNR/SNDR/SFDR (dB)	67/66/75	67/66/75	75/-/88	67/63/67	64/62/68
First Integrator Gain (dB) / Current (mA)	26 / 2	26 / 2	-/10	-	54/-
First Integrator Topology	Diff-pair	Diff-pair	Folded Cascode	Gm-C	Telescopic
Sampling Freq (MHz)	150	150	80	160	360
Calibration Filter Order	8-tap FIR (sign-data LMS)	8-tap FIR (sign-data LMS)	6tap FIR (LMS)	6-tap FIR (Var. Est)	IIR (LMS)
Power(analog) mW (digital) mW	31.5 54 (FPGA)	31.5 38 (FPGA)	185 55	104 14.4	183 47
Area (analog) mm^2 (digital) mm^2	1.73 3915 ALUT	1.73 5431 ALUT	2.5 1.5	1.7 0.09	0.68 0.59
Tech	0.13 µm CMOS/ Altera Stratix-II	0.13 µm CMOS/ Altera Stratix-II	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS

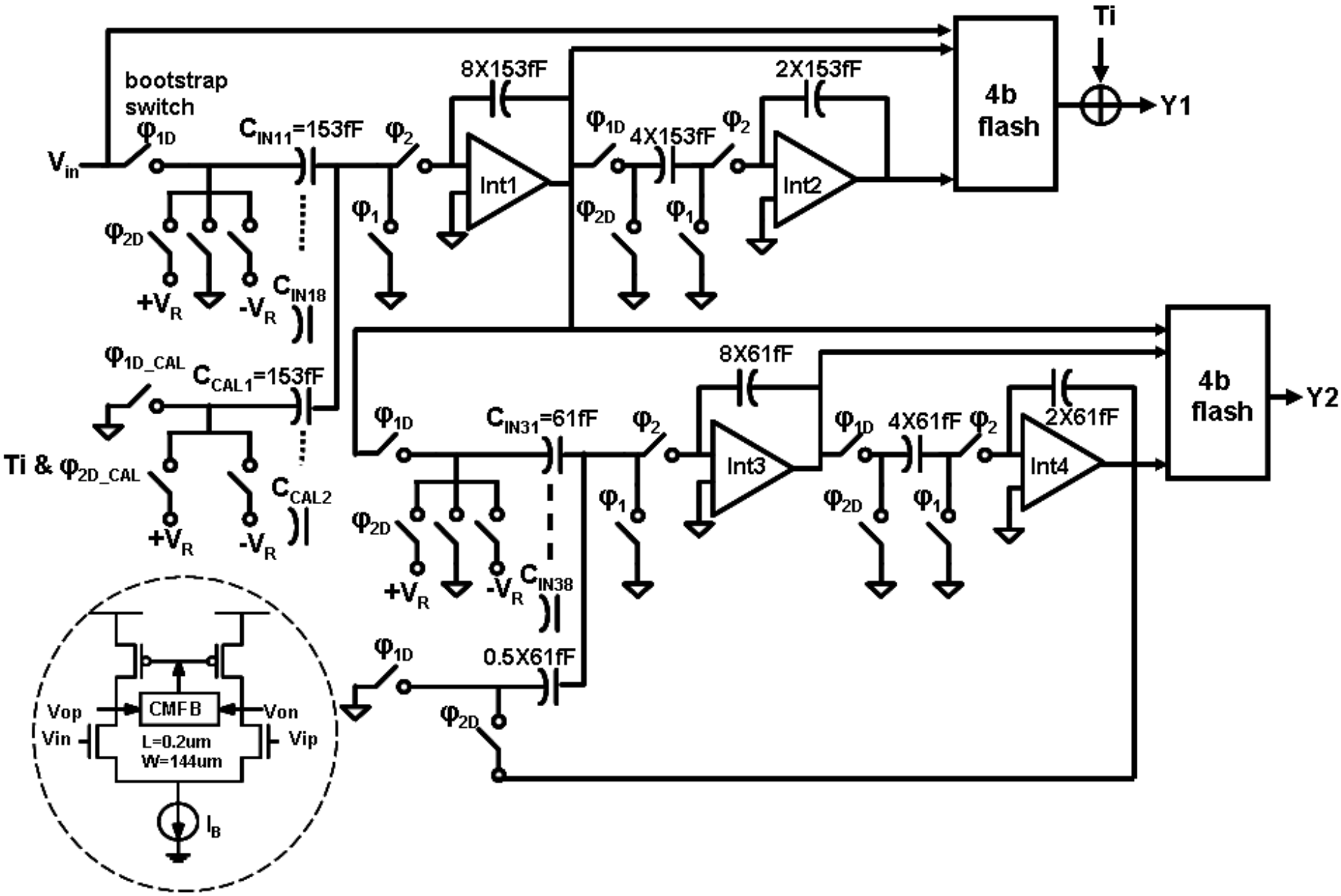
Conclusions

- Demonstrated use of 26-dB gain opamps in ΣΔ ADCs
- LMS calibration to recover from gain errors in cascade ADCs
- Proposed half-rate and quarter-rate polyphase decomposition schemes for LMS-calibrated ΣΔ ADCs
- Polyphase decomposition schemes reduce power consumption for high-frequency, wide-bandwidth applications

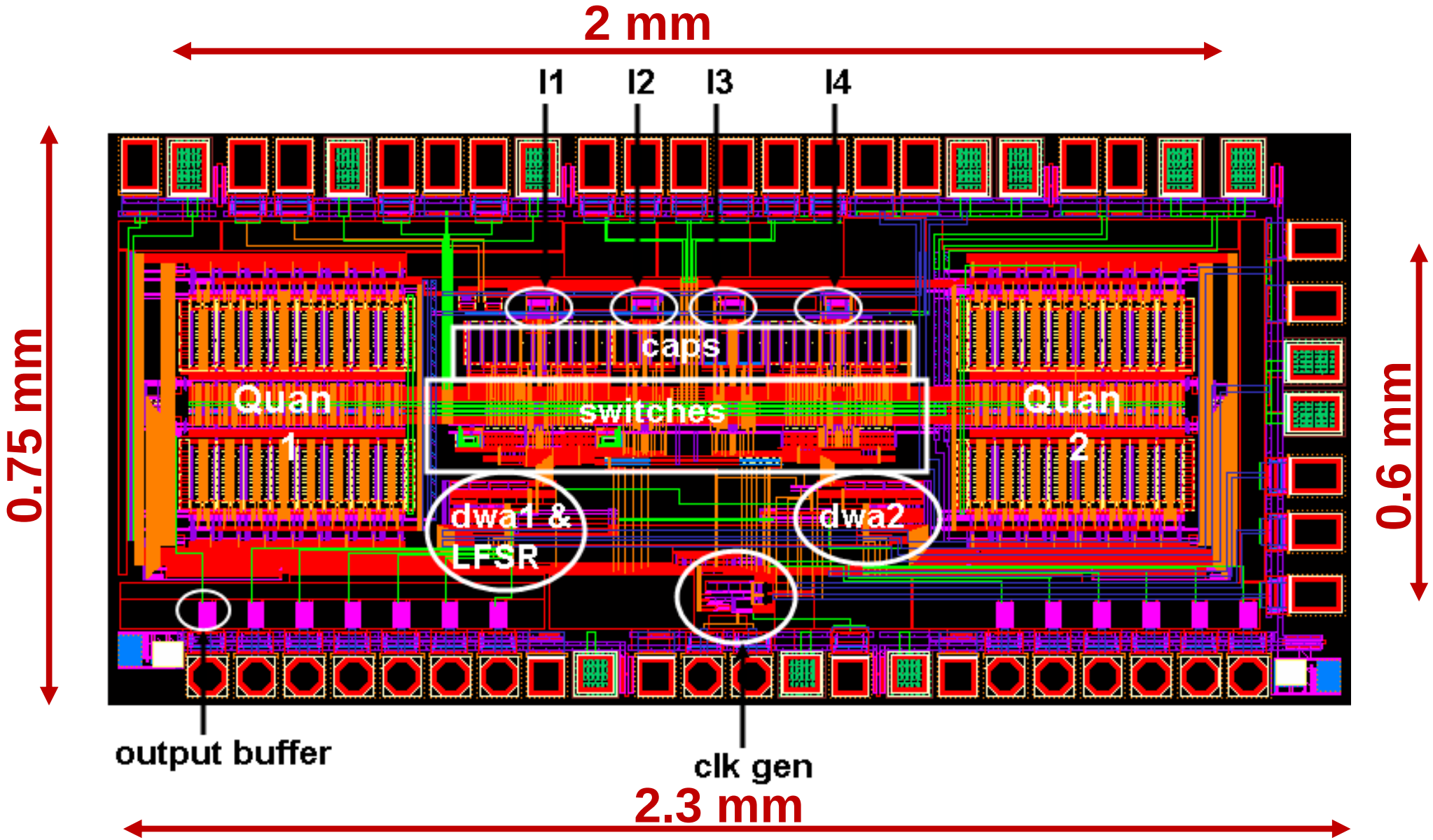
THANK YOU

Questions?

Switched-capacitor implementation of 2-2 ADC



Chip Layout


2 mm
I1
I2
I3
I4
0.75 mm
caps
Quan
1
switches
Quan
2
0.6 mm
dwa1 &
LFSR
dwa2
output buffer
clk gen
2.3 mm

Chip Micrograph